ABSTRACT OF THE DISCLOSURE

An FET is connected between the emitters of first and second transistors. The emitter of the first transistor is connected to a ground terminal through a plurality of resistors and the emitter of the second transistor is connected to the ground terminal through a plurality of resistors. Another FET is connected between a node between the plurality of resistors on one side and a node between the plurality of resistors on the other side. The gates of the FETs are connected to a control terminal receiving a control voltage through resistors respectively. The resistors and the FETs form a variable resistance circuit. Alternatively, two FETs are serially connected between nodes connected to the emitters of the first and second transistors. Another FET is connected between a node between the two FETs and a ground terminal. The gates of the two FETs are connected to a control terminal receiving a control voltage through resistors respectively. The gate of the other FET is connected to a control terminal receiving a control voltage through a resistor. The control voltages change complementarily to each other. The FETs form a variable resistance circuit.